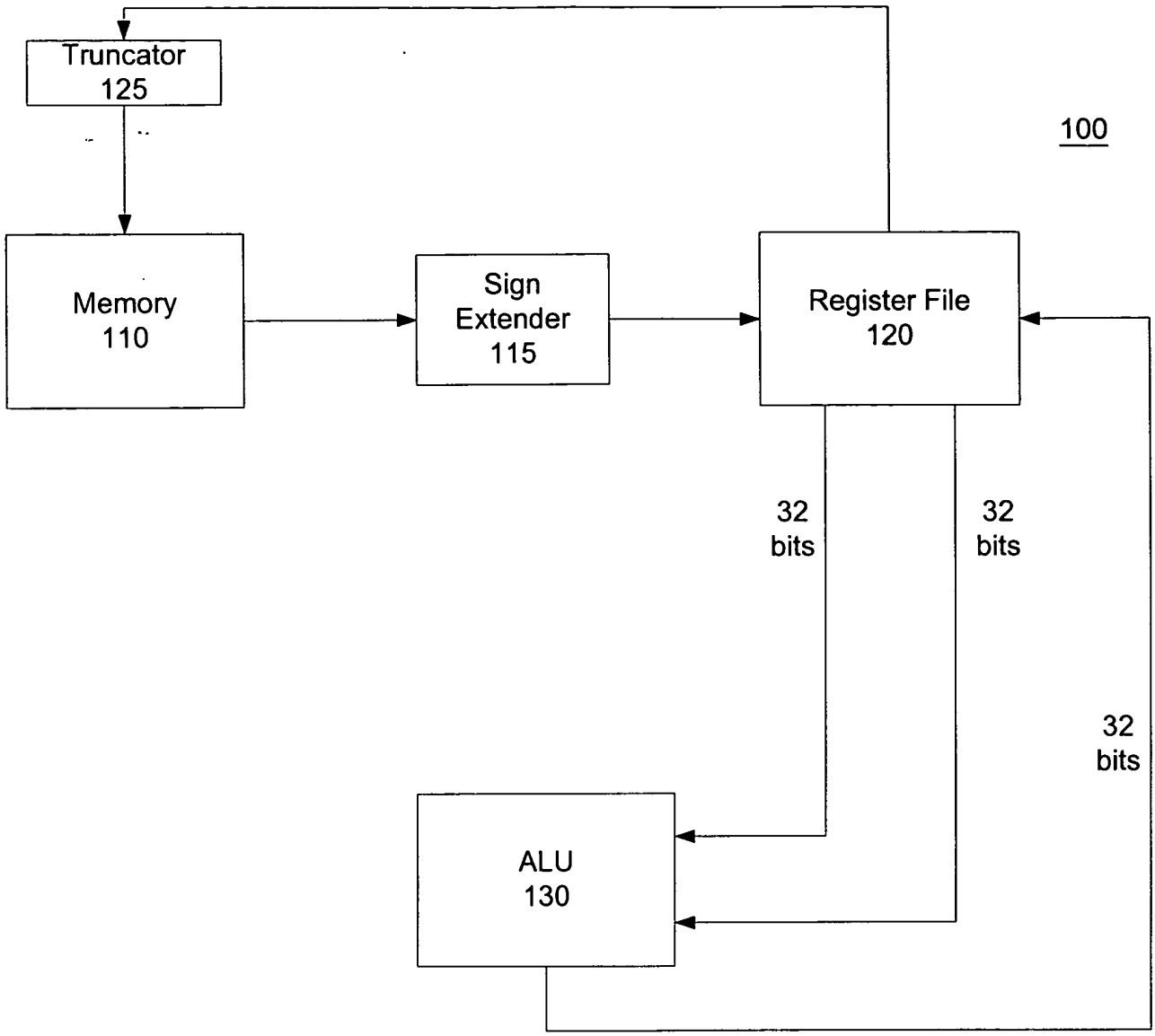

Figure 1A

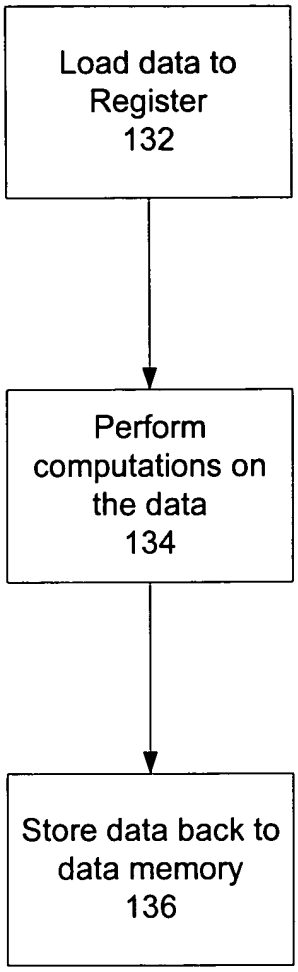
Load data to Register 132
Perform computations on the data 134
Store data back to data memory 136

Figure 1B

OPCode 6 bits	Source1 Register 5 bits	Source2 Register 5 bits	Target Register 5 bits	Sub-OPCode 11 bits

Figure 1C

OPCode 6 bits	Target Register 5 bits	Source1 Register 5 bits	Immediate 16 bits

Figure 1D

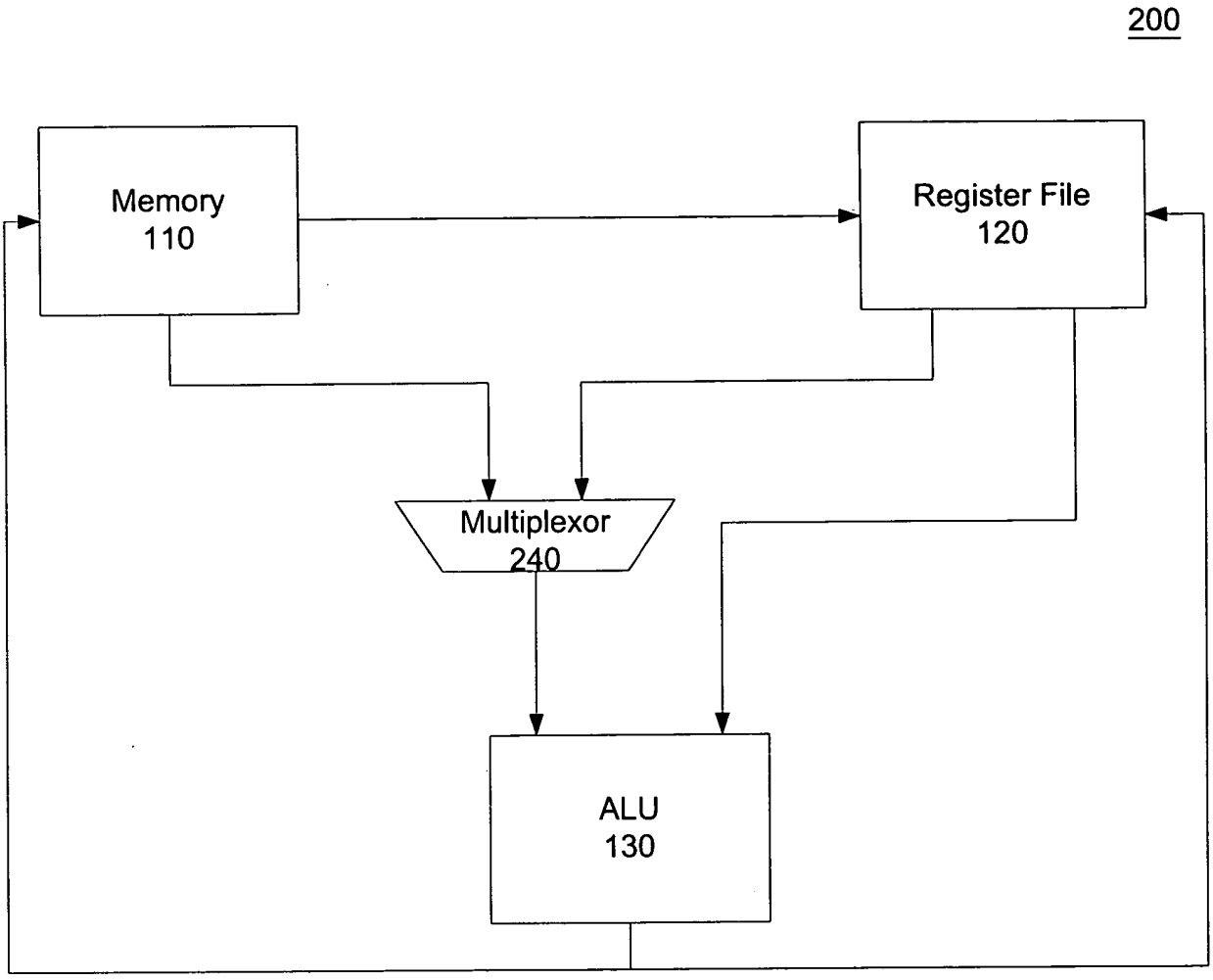

Figure 2

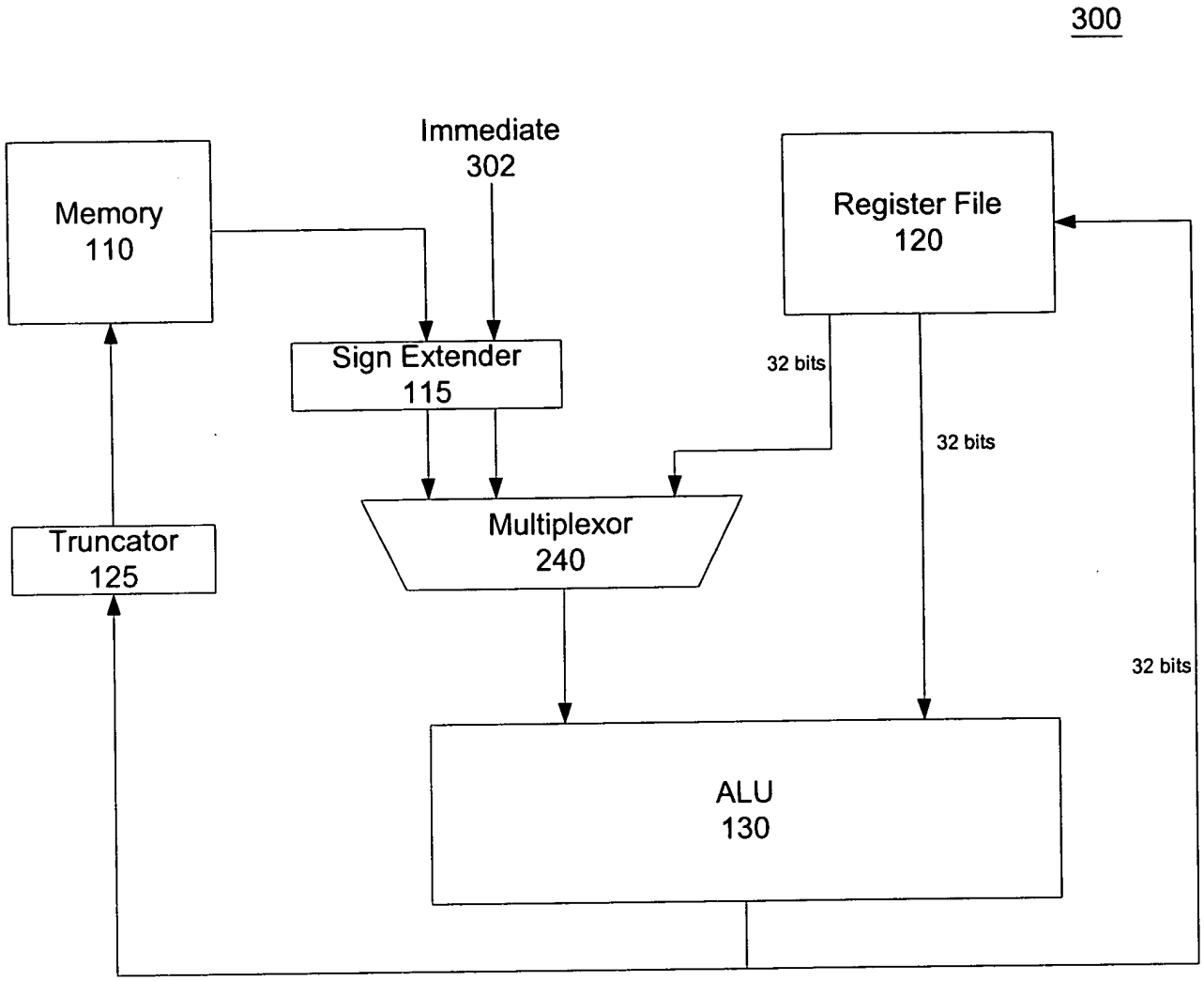
300
Immediate
302
Memory
110
Register File
120
Sign Extender
115
32 bits
32 bits
Multiplexor
240
Truncator
125
32 bits
ALU
130

Figure 3A

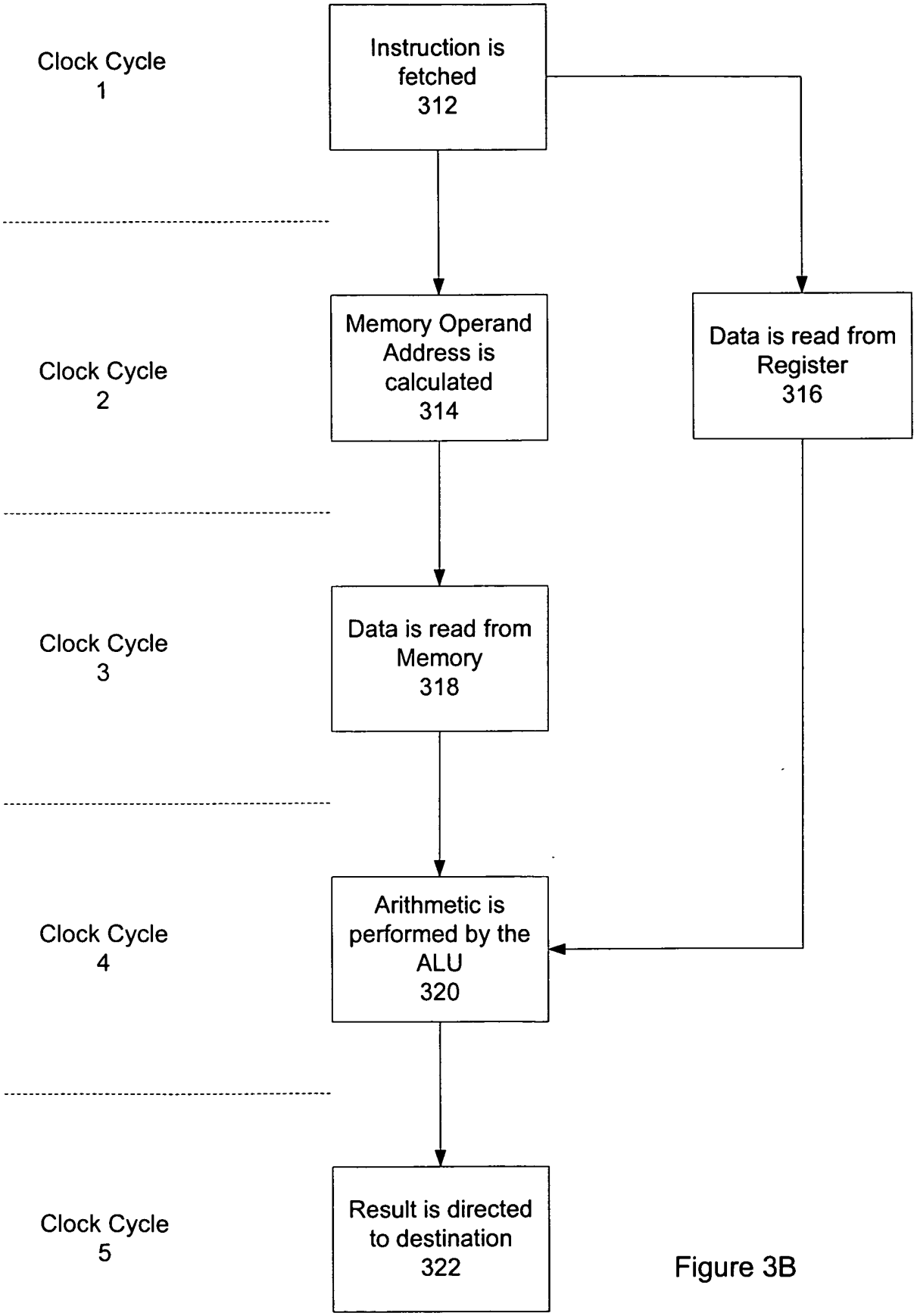

Figure 3B

400

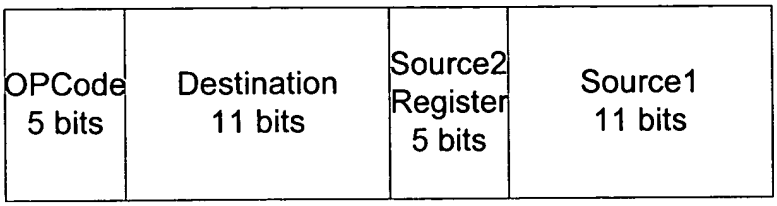

Figure 4

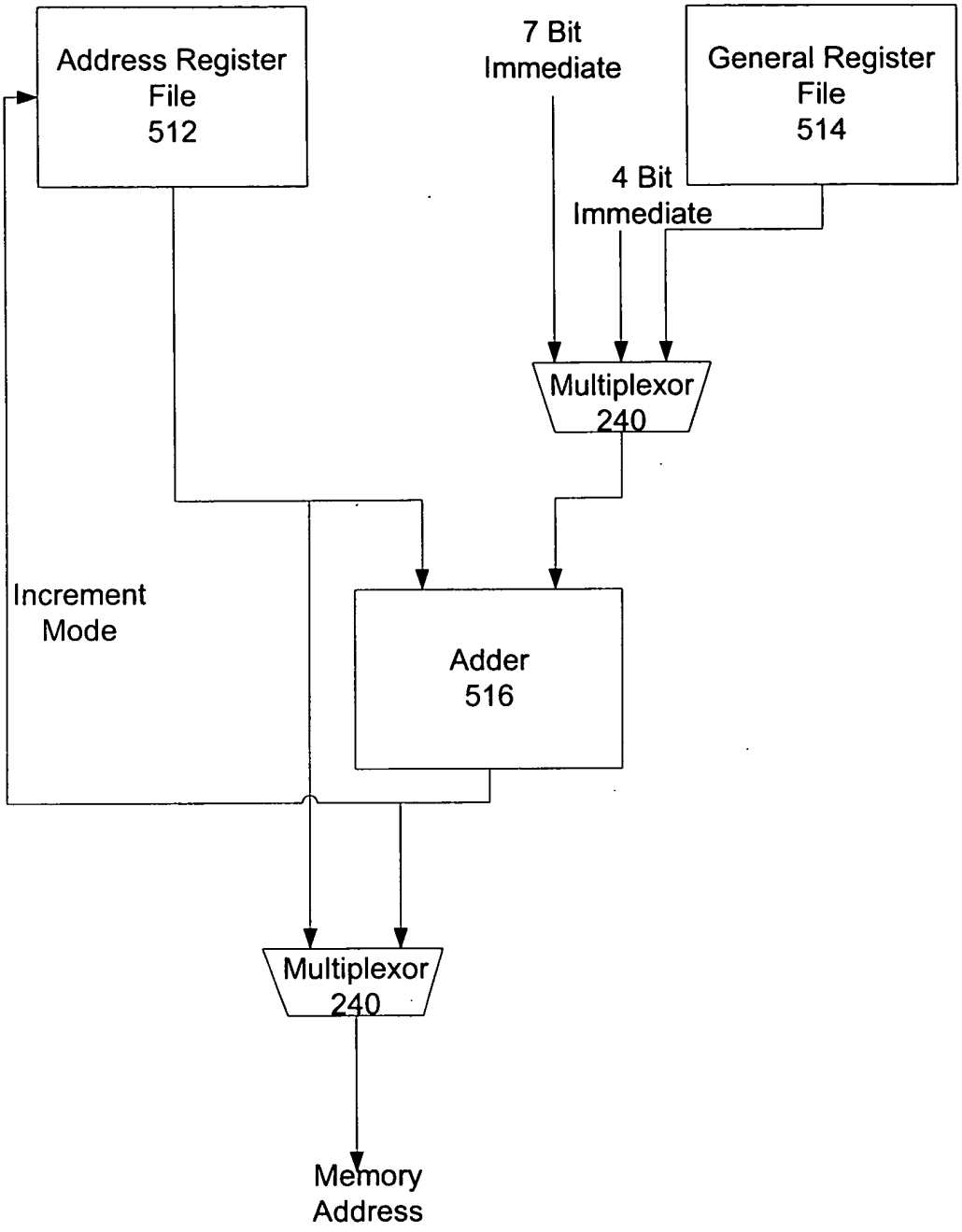

Figure 5

<table>
<tr><td>1</td><td>I_6 I_5</td><td rowspan="3">$A_2A_1A_0$</td><td colspan="5">I_4 I_3 I_2 I_1 I_0</td><td>Row 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td colspan="5">R_4 R_3 R_2 R_1 R_0</td><td>Row 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>M</td><td colspan="4">I_3 I_2 I_1 I_0</td><td>Row 3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td colspan="6">Register Direct</td><td>Row 4</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td colspan="6">Immediate</td><td>Row 5</td></tr>
</table>

Figure 6

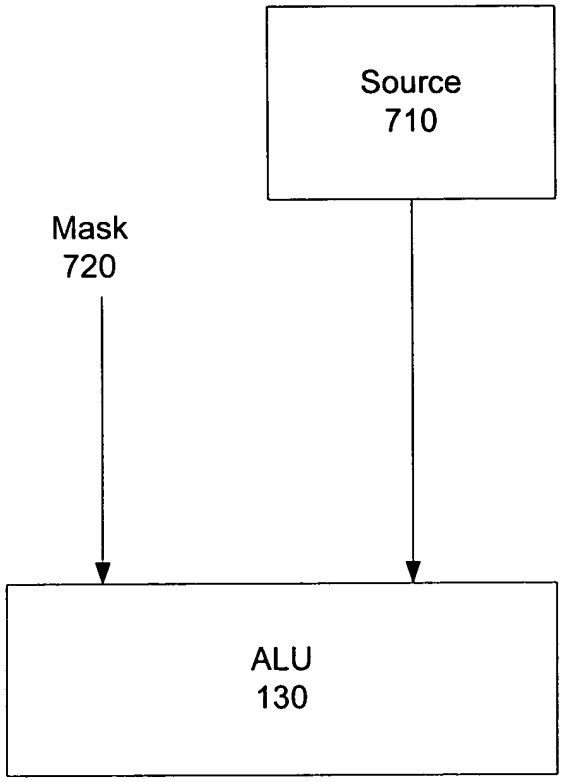

Figure 7

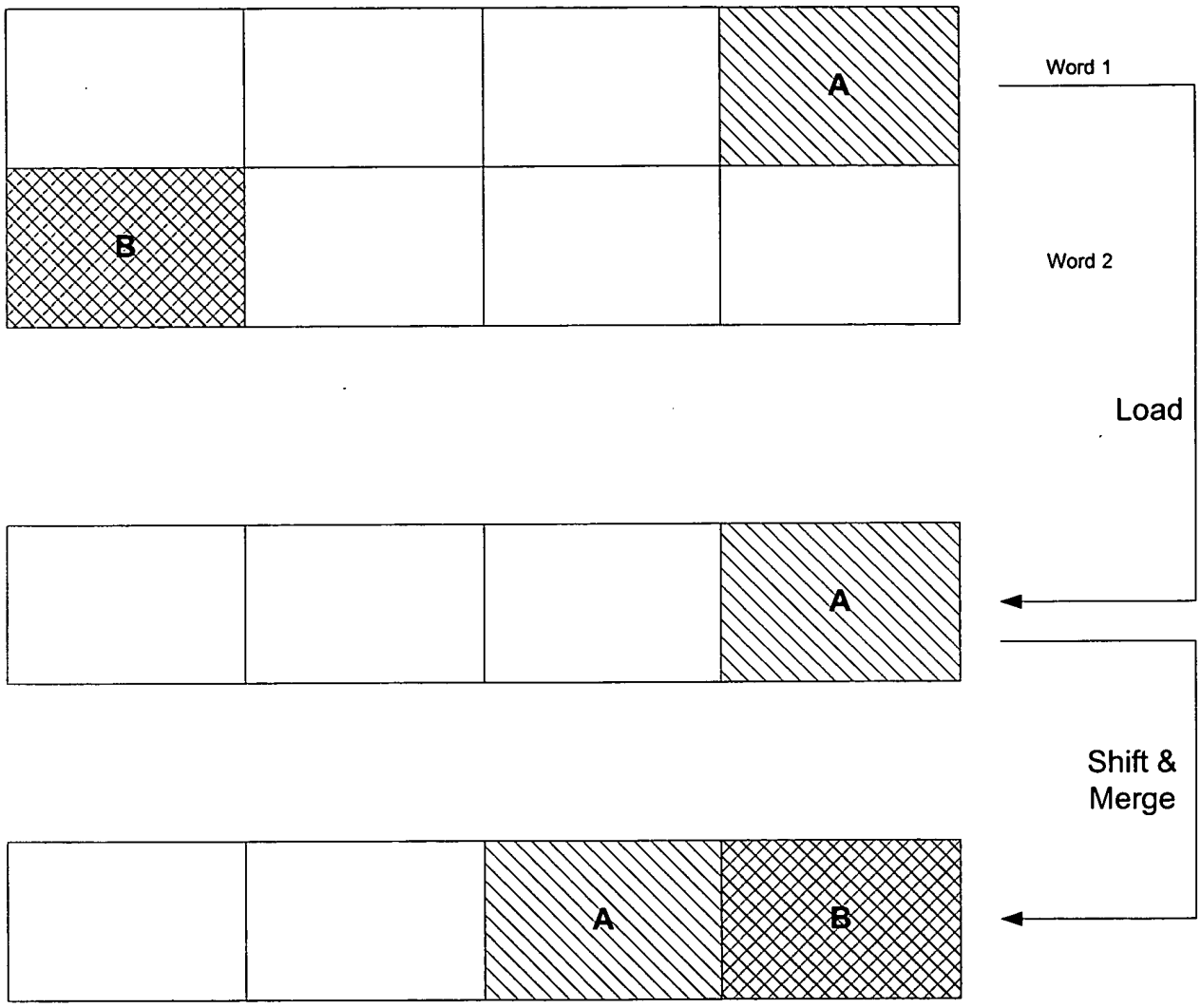

Figure 8

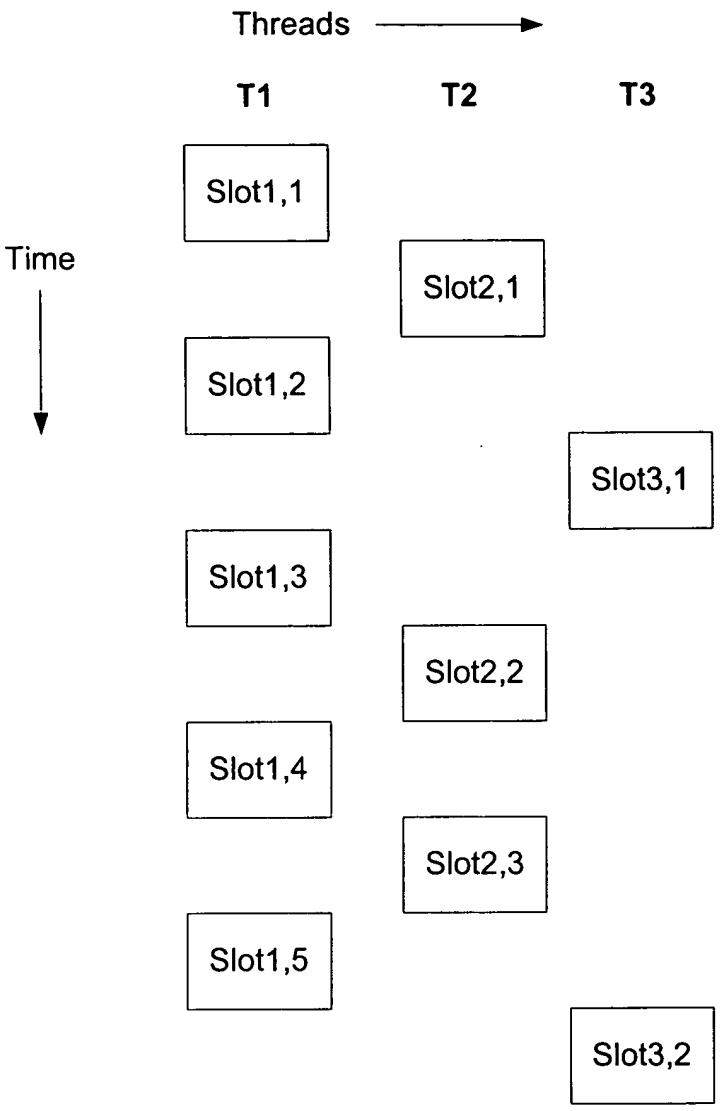

Figure 9